

APPLICATION NOTE

**- TDA9901 -
DIGITAL PROGRAMMABLE GAIN
AMPLIFIER**

**DEMONSTRATION BOARD
AN/98105**

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AMPLIFIER**

DEMONSTRATION BOARD

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SUMMARY

This Application Note describes the design and the realization of the **DEMO9901** Demonstration board using a **TDA9901** with an application environment. The **TDA9901** is a Digital Programmable Gain Amplifier (DPGA). In order to obtain the best performances, all the main recommendations which have to be applied to design the Printed Circuit Board are also described.

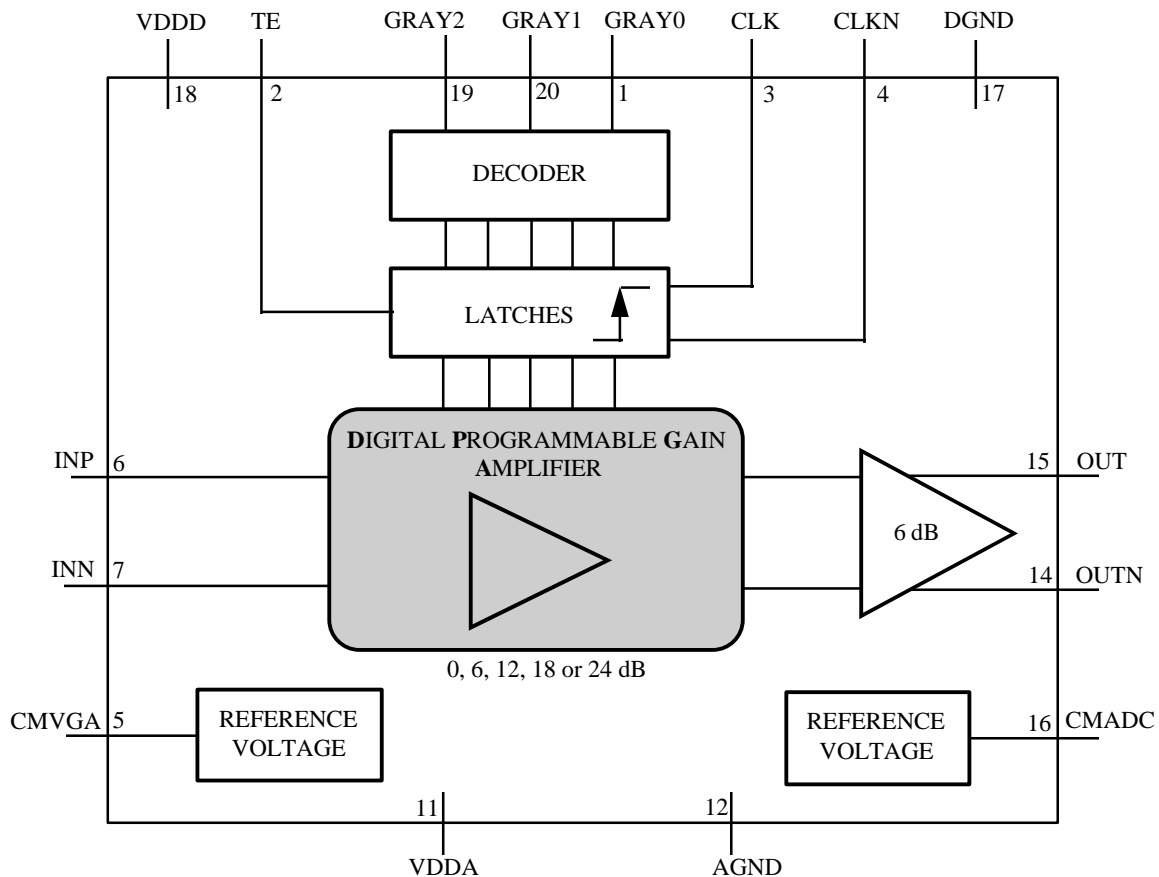
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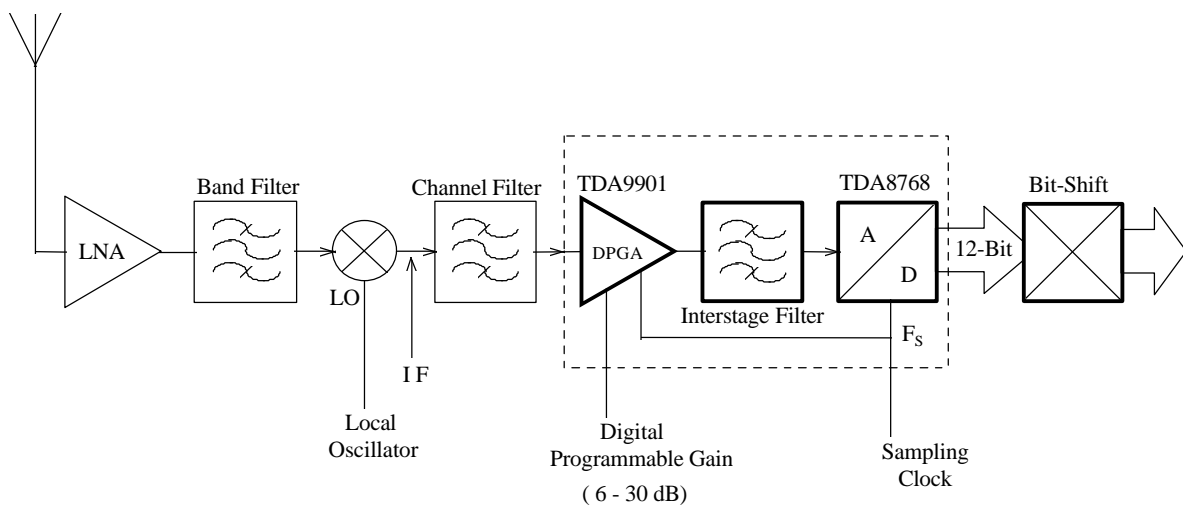
1. MAIN FEATURES OF THE TDA9901

The **TDA9901** whose the block diagram is shown on **Figure 1**, is a monolithic BICMOS low noise, wide-band amplifier with differential inputs and outputs. This product can work in Latched mode or Transparent mode under a single 5V supply voltage with a typical consumption of 150mW only. Therefore, the Digital part of the device can be supplied under a reduced supply voltage of 3.3V.

The **TDA9901** incorporates an AGC function operational between a gain of 6 to 30dB thanks to five CMOS compatible digital control steps (*from 3-bit GRAY code*) which can operate in transparent mode (*direct control of gain setting*) or in latch mode (*gain setting controlled by latch signal*). The **TDA9901** is optimized for quick-change of gain settings while preserving a small phase and small amplitude error. Moreover, this device presents an excellent combination of the Noise Figure and good linearity for a wide input frequency range. Therefore this device can be used as simple Multi-purpose amplifier or still in the Linear AGC systems or in the professional application domains such as Radio communications, instrumentation, etc...



The **TDA9901** is optimized for processing IF signals in Global System for Mobile communications (*GSM*) Base-Stations or satellite receivers whose the basic architecture of the wideband receiver is shown **Figure 2**.



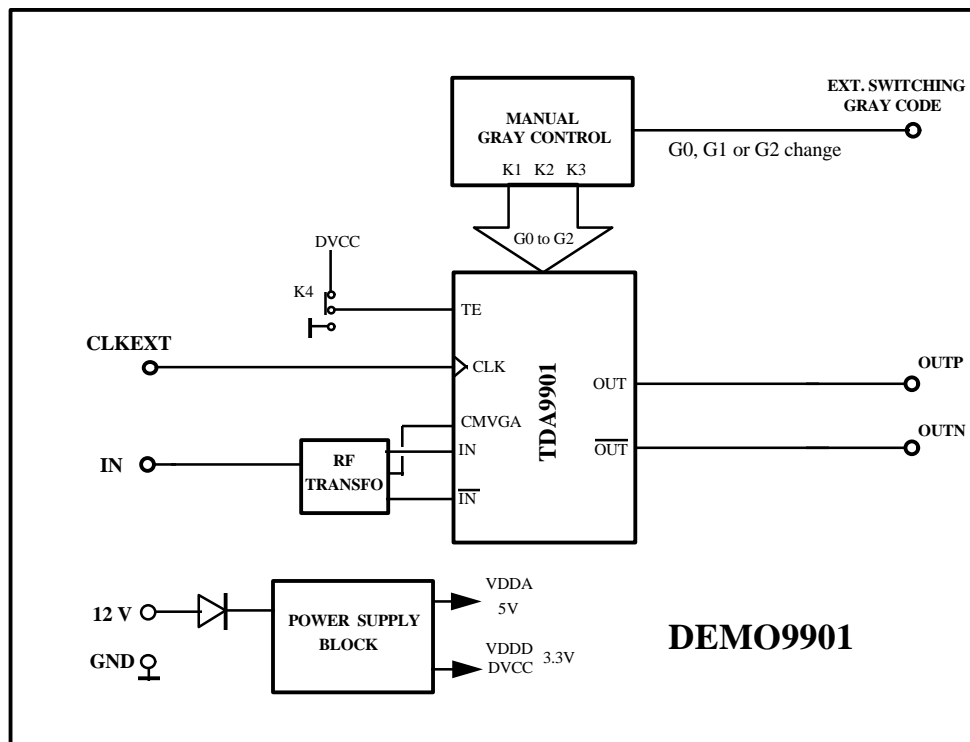
- FIGURE 2 -

Indeed, thanks to a large bandwidth (*125MHz at -3dB cut-off frequency*) and dynamic gain, the **TDA9901** can drive the analog inputs of an ADC in order to increase and to obtain the required dynamic range of the channels before to Analog to Digital Conversion system.

On the other hand, in order to reduce the number of external components required and system cost, the **TDA9901** was designed to be easily usable with the 12-bit Analog to Digital Converter type TDA8768 of Philips Semiconductors. In fact, it generates its proper common mode input DC voltage level but also the input DC common mode voltage of the TDA8768.

2. PRINCIPLE AND DESCRIPTION

The principle of the Demonstration board, which is described in this Application Note, is shown on **Figure 3**. The electrical diagram, the part list associated with the implementation scheme are given in the "**Demoboard file**" chapter of this Application Note.



- FIGURE 3 -

The different blocks constituting the board are the following :

- **A power supply** constituted by a low power voltage regulator, to supply the DVCC, VDDA, VDDD on all circuitry on the board.
- **A 50Ω RF transformers** to transform the analog signal applied on the "IN" 50Ω SMA connector to symmetrical differential mode on the analog inputs INP and INN of the amplifier.
- **A manual Gray control block** to address the static voltage levels on the Gray inputs of the amplifier.

- **A TDA9901 Digital Programmable Gain Amplifier** used to amplify the analog signal applied on the "IN" 50Ω SMA connector.
- **A dynamic Gray input** with "GRAY" 50Ω SMA connector to change only one bit among three (*code Gray definition*).
- **An external clock input** with "CLKEXT" 50Ω SMA connector to control the gain in latched mode.

The Demonstration board is functional with a single + 8 to 12 Volts external power supply and the different digital input compatibilities are mentioned in the following table :

CLKEXT	GRAY
PECL TTL CMOS or LV-CMOS AC coupling SINEWAVE	TTL or CMOS

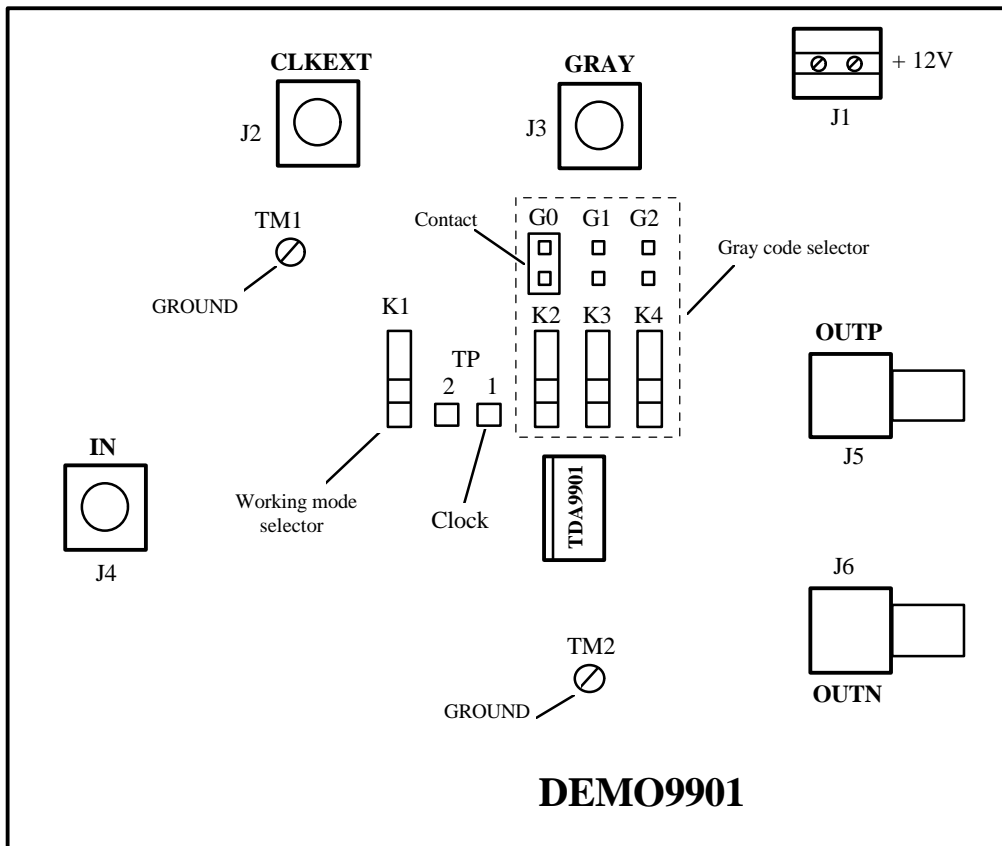
In latched mode ($TE = 0$) the clock signal is external from a 50Ω generator applied on the "CLKEXT" 50Ω SMA connector. **In this case, the gain change is fixed at the rising edge of the clock signal.**

In transparent mode ($TE = 1$) In transparent mode, the dynamic clock signal is not necessary, **the gain change is directly controlled by the Gray input data pattern when the clock signal is high.**

Remark : *In transparent mode, in order to limit the Electro-Magnetic Interferences level it is advised to take disable the clock source and replace this by a simple high DC level (between 2V to VCC value).*

3. OVERALL VIEW OF THE BOARD

The whole layout of this Demoboard is shown in **Figure 4**.



- FIGURE 4 -

The different connection plugs, switches and test-points available on the board are, for :

*** General power supply**

- A connector **J1** type Phoenix to connect the Demonstration-Board to an external power supply between + 8 V to 12 V and **GND**.

*** Evaluation of the TDA9901**

- One analog input **IN** with 50Ω SMA connector **J4** to connect the single-ended analog signal applied on the input RF transformer, used to produce a symmetrical differential signal applied on the DPGA.

- One external clock input **CLKEXT** with 50Ω SMA connector **J2**, associated at two test points TP1/2 to display the clock signal.
- One external dynamic Gray input **GRAY** with 50Ω SMA connector **J3** associated to three contact **G0**, **G1** and **G2** to change dynamically one bit among the three (*G0*, *G1* and *G2*).
- Three switches **K2** to **K4** to address the static logic level applied respectively on Gray code input pins G0, G1 and G2 of the DPGA in order to obtain the desired differential gain corresponding to the following table :

GRAY INPUT DATA CODE			GAIN (dBV)
G0	G1	G2	
0	0	0	6
1	0	0	12
1	1	0	18
0	1	0	24
0	1	1	30

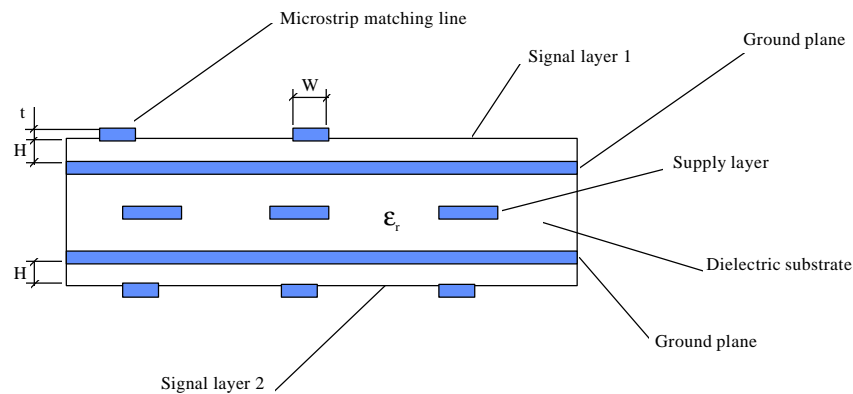
- One switch **K1** to choose the Transparent or Latched working mode corresponding to the hereunder table :

TE	WORKING MODE
0	LATCHED
1	TRANSPARENT

- Two outputs **OUTP** and **OUTN** with two SMA connectors **J5** and **J6**
- Two ground connections **TM1** and **TM2**.

4. TECHNOLOGICAL CONCEPT

The practical design has been made on a multilayer **P**rinted **C**ircuit **B**oard of 3.0" x 2.7" size. The technological concept chosen to make this multilayer PCB uses five physical layers as shown **Figure 5**. The first and fifth layers are the signal layers, the second and fourth layers constitute the ground planes corresponding to signal layers. Moreover, the third layer situated between two ground planes has been provided especially to design the power wiring system.



- FIGURE 5 -

The dielectric substrate used is an Epoxy Glass resin having a relative permittivity of 4.7 and a copper thickness (t) of 35 μm . The metallized via hole technic was employed to make all necessary interconnections between layers. The global thickness of the PCB is about 64 mils (1.6 mm) with a thickness (H) between signal layers to respectively ground of 8 mils (0.2 mm). So, all the 50 Ω matched lines were designed with the microstrip technology and the width ($W=12.7$ mils) of these lines determined from the Kaup's relation :

$$W = \frac{7.475H}{\exp(Z_C \sqrt{\epsilon_r + 1.41} / 87)} - \frac{t}{0.8}$$

Taking into account low switching current in the digital part of the TDA9901 is not necessary to use two separate digital and analog ground planes. On the Demonstration-Board a structure with an electrical single ground was adopted. To avoid ground planes discontinuities of the line technological structure, the supply wiring system of all circuitry has been made on the internal third layer. Moreover, in order to reduce the voltage fluctuation effects, the DC supply currents are driven to the devices by very low characteristic impedance microstrip lines having a small equivalent inductance.

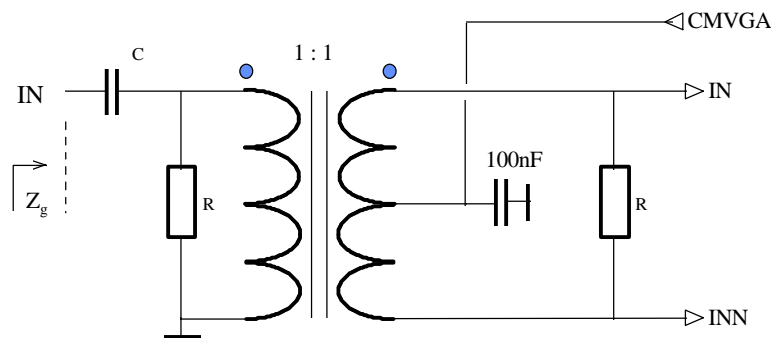
On the other hand, in order to satisfy the **E**lectro-**M**agnetic **C**ompatibility requirements and to ensure a good Power Supply Rejection Ratio on the different supply pins and to suppress an eventual close-in coverage risk, each supply line close to DPGA is wideband bypassed (*see Chapter 5 § 3*).

5. SPECIAL FEATURES OF THE TDA9901

In order to obtain the optimal performances, the advised Application scheme of the TDA9901 is shown on the **Figure 25** on the "Demoboard file" chapter. However, several requirements must be satisfied about the following specific points described in this chapter.

5.1 ANALOG INPUT OF THE AMPLIFIER

In order to improve the analog signal to noise ratio, a differential structure with an intrinsic low input offset voltage was designed on the TDA9901 analog input. A wideband RF transformer is used to make the adaptation between the single-ended Analog input of the Demonstration-Board and the differential analog inputs of the DPGA as shown on **Figure 6**.



- FIGURE 6 -

The recommended **DC common mode voltage** is internally fixed on the DPGA analog inputs IN and INN from the 2.7V internal reference voltage available on the CMVGA pin . A frequency decoupling of maximum 100nF was added on the middle point of the transformer secondary, to get a good "dynamic" ground.

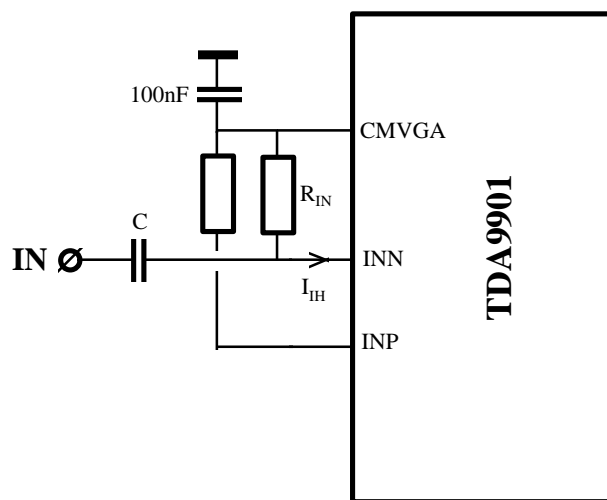
The dynamic analog signal is connected through a 220nF AC coupling to the input RF transformer via a short 50Ω microstrip matched line and a SMA plug-in connector. In fact, in order to preserve a good signal to noise ratio, a recommended low impedance matching must be located at the input transformer. So, the symmetrical and differential analog signal is applied on the analog inputs INP and INN of the DPGA. The secondary load R of the RF transformer was fixed to 100Ω in order to ensure a 50Ω matching with regard to an **analog virtual ground**. Thereby, with a transformer ratio of $n=1$, the impedance brought back at the primary is equal to R value and the impedance matching to the external generator is performed with a resistor of 100Ω in parallel on the primary of the transformer. The combination of the capacitor C and the equivalent impedance ($R/2$) located on primary transformer form a high-

pass filter whose the -3dB cut-off frequency is determined by following equation : $F_{3dB} = 1 / p R C$.

Note : On the other hand, by the using of a transformer ratio (n) higher than unity, the brought back impedance Z_b at the primary is given by following relation :

$$Z_b = R / n^2$$

Note : The Digital Programmable Gain Amplifier TDA9901 can be used with a single-ended AC coupled analog input, in this condition the proposed diagram is shown on **Figure 7**.



- FIGURE 7 -

In order to reduce the input noise, it is advised to employ a low R_{IN} value. Therefore, in order to limit the offset voltage between the differential inputs of the device, the R_{IN} value will must be computed taking into account the maximum absorbed analog input current value ($55\mu A$).

In this condition the true common mode voltage value V_{ICOM} obtained on the differential inputs is given from the relation :

$$V_{ICOM} = V_{CMVGA} - R_{IN} \cdot I_{IH} .$$

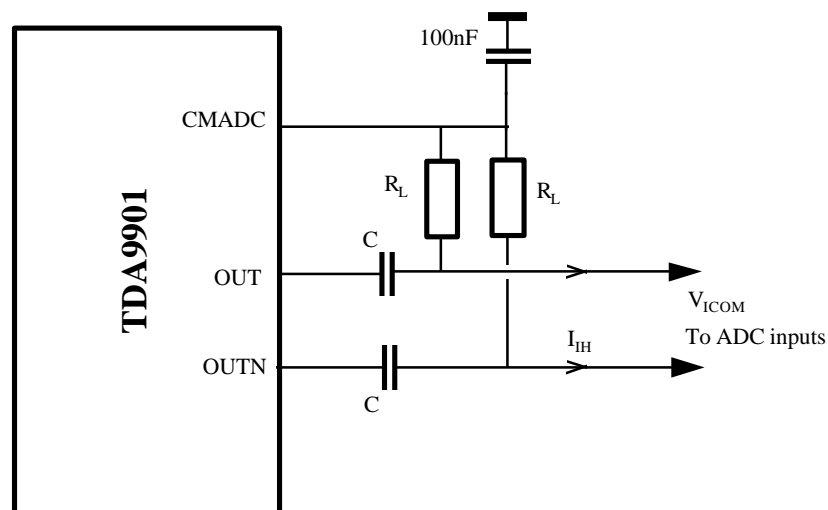
The combination of the capacitor C and resistor R_{IN} form a high-pass filter, consequently, the following condition $1 / C \omega \ll R_{IN}$ must be respected for the whole analog bandwidth.

5.2 REFERENCE VOLTAGES

In order to reduce the complexity of the systems, two reference voltages are designed inside the device. These reference voltages are directly available on specific output pins CMVGA and CMADC with a respectively typical regulated voltage value of 2.7 and 3.54 Volts.

As shown **Figures 6 and 7**, the internal reference voltage **CMVGA** of 2.7V is used to ensure the Common Mode Voltage on the analog inputs of the TDA9901. The output pin CMVGA will be wideband bypassed with a minimum capacitor value of 100nF.

The output reference voltage **VCMADC** of 3.54V supplied on CMADC pin of the device, can be used when the Digital Programmable Gain Amplifier TDA9901 will drive, a differential analog input signal to TDA8768 Analog to Digital Converter of Philips Semiconductors as shown **Figure 8**.



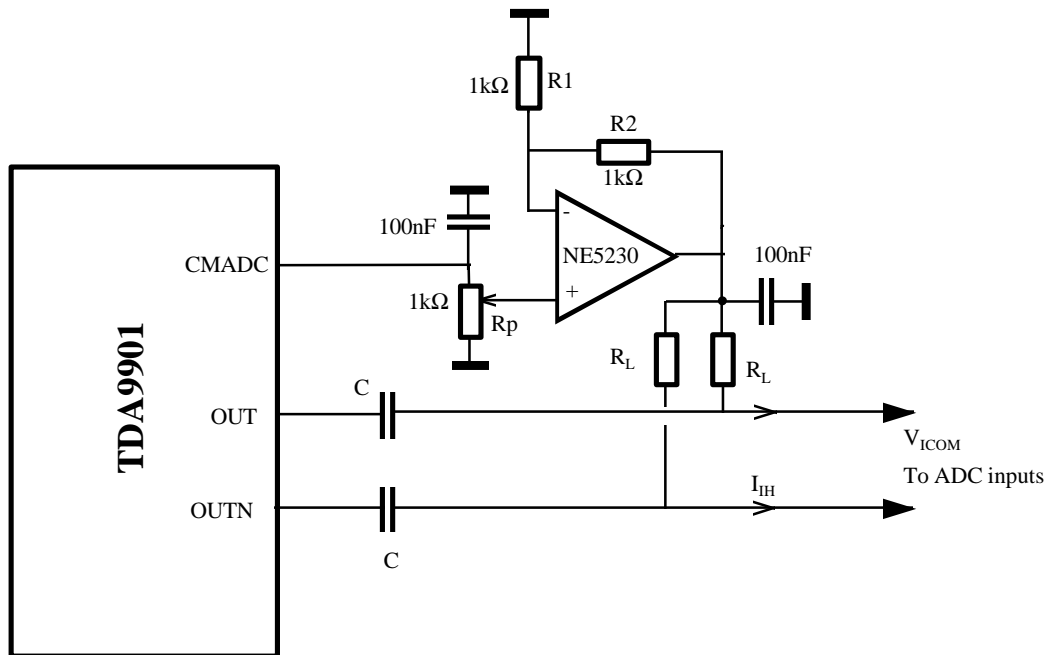
- FIGURE 8 -

The output signal is AC coupling on the ADC inputs, consequently, the reference voltage V_{CMADC} ensures the common mode voltage V_{ICOM} of the differential analog inputs of the TDA8768 through the dynamic load R_L of the device.

Taking into account high level analog input current I_{IH} of the TDA8768 (*about published typical value 10 μ A*), the common mode voltage V_{ICOM} can be evaluated from the relation :

$$V_{ICOM} = V_{CMADC} - R_L \cdot I_{IH}$$

Note : The TDA9901 can drive an other ADC that TDA8768, in this case, an other common mode voltage will can be required. Consequently, the hereunder diagram shown **Figure 9** can be realized in order to obtain the required common mode voltage value.



- FIGURE 9 -

Indeed, the reference voltage V_{CMADC} supplied from TDA9901 is used as reference source to create an other reference voltage V^+ , which can be adjusted thanks to potentiometer R_p on the no-inverter input of the single supply Operational Amplifier type NE5230 of Philips Semiconductors.

Consequently, we have :

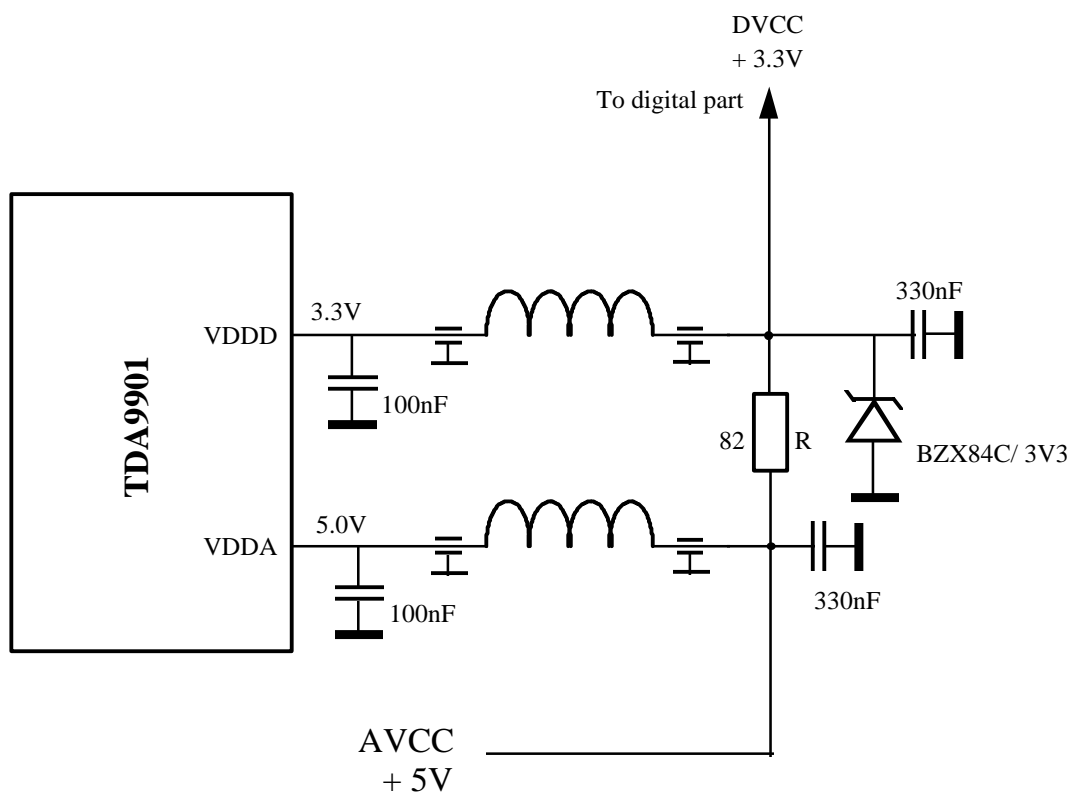
$$V^+ = k \cdot V_{CMADC} \quad \text{with} \quad 0 < k < 1$$

The Op Amp. is powered from +5V supply, with a non-inverting DC gain of 2. Consequently, the common mode voltage V_{ICOM} obtained on the resistor load R_L is given from the following relationship :

$$V_{ICOM} = k \cdot V_{CMADC} \cdot \left(\frac{R1 + R2}{R1} \right) - R_L \cdot I_{IH}$$

5.3 ANALOG AND DIGITAL POWER SUPPLIES

In order to obtain a good dynamic rejection on the DPGA supply pins, the Analog VDDA and Digital VDDD supply lines are addressed to the supply pins, of the DPGA, through two SMD bypass pi filters as shown by the schematic supply diagram of **Figure 10**.



- FIGURE 10 -

These bypass pi filters are implanted near the DPGA to separate each power supply of the device. Moreover, the PCB layout has been designed so that the power supply line end arrives close to the VDDA and VDDD sides. These points are perfectly decoupled with 330nF and 100nF ceramic capacitors close to respective supply pin of the device. On the Demonstration-Board, the digital part of the device is supplied under VDDD of 3.3V from stabilized voltage DVCC obtained from a Zener diode type BZX84C/3V3 of Philips Semiconductors.

Therefore, in order to ensure a good stability on DVCC and VDDD voltages, a resistor R allows to limit the current in Zener diode at about to ten times as big than digital consumption of the device.

5.4 CLOCK INPUT

In order to obtain a changing gain in latched mode, the TDA9901 must be used with an clock signal. The differential clock inputs of the device are internally biased to ensure a TTL compatibility with a threshold voltage about 1.4V and a large equivalent input impedance (*higher than 100k Ω*). In fact, a flexible clocking compatibility is possible with of simple interface circuits.

Consequently, the DPGA can work also with Logic Standard PECL or with the minimum condition AC driving mode as mentioned in the following table :

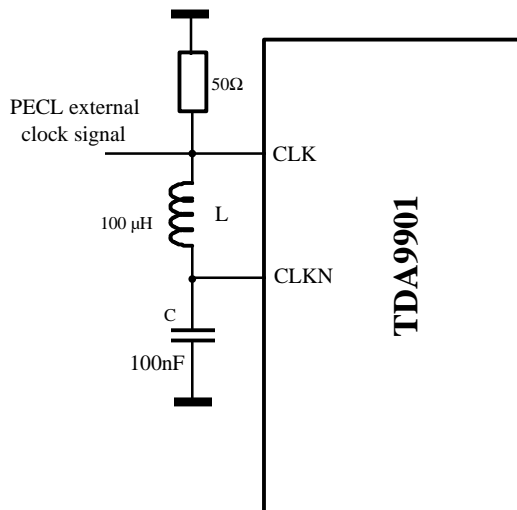
MODE	CLK	CLKN
PECL	PECL	3.65 V (DC)
	3.65 V (DC)	PECL
	PECL	PECL
AC	0.5 V _{p-p}	2.5 V (DC)
	2.5 V (DC)	0.5 V _{p-p}
	0.25 V _{p-p}	0.25 V _{p-p}

The required PECL limit levels and AC amplitude on the clock pins of the device are the following :

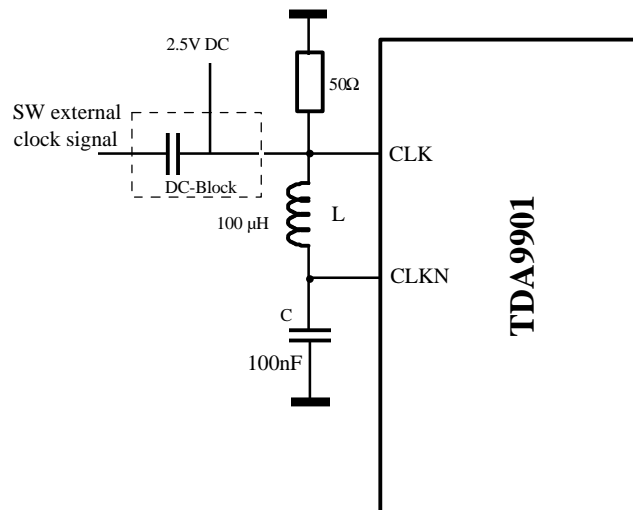
MODE	V _{IL}	V _{IH}
PECL	3.52 V	3.83 V
AC	0.5 V p-p	

When TTL or PECL clock signal is used, in order to reduce the Electro-Magnetic Interference Bandwidth, it is preferable to limit the clock transient values (*rise and fall time higher than 0.75ns*). In fact, in **Radio communication Applications** where an effective reduction of the Spurious Free Dynamic Range (*SFDR*) is very important, an AC coupling Sinewave clock signal is advised.

The Demonstration-Board is designed to be functional in latched mode with a single-ended DC coupled PECL or TTL clock signal from an external 50Ω generator as shown **Figure 11**.



- FIGURE 11 -



- FIGURE 12 -

The DC offset voltage is restored on the CLKN pin from the average PECL level, thanks to a Low-pass filter LC. In order to ensure a good dynamic rejection on complementary clock input a high inductance value ($100\mu H$) associated to the decoupling capacitor C, is required.

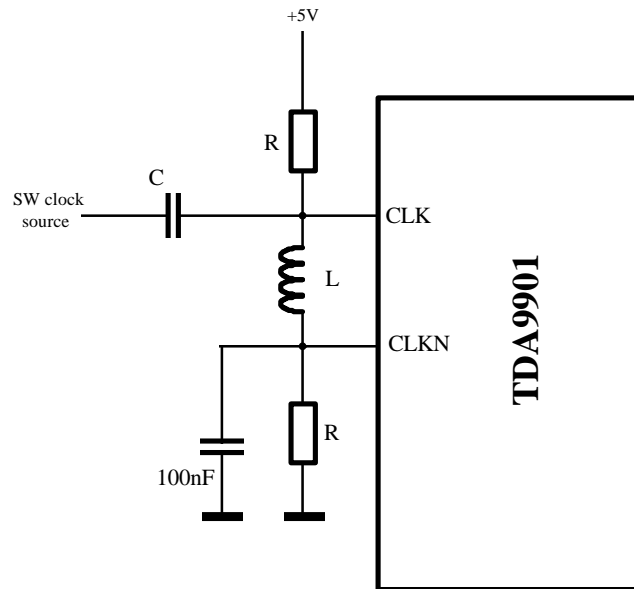
In order to ensure a good matching of the 50Ω external generator at the clock frequency (F_c), the following condition must be respected :

$$L \omega_c \gg 50W$$

On the other hand, to obtain an AC coupling clock mode from an external Sinewave 50Ω generator as shown **Figure 12**, it is possible to add an external DC-block on the CLKEXT of the Demonstration-Board. This will be connected to an external voltage source of 2.5V to ensure the offset voltage required with this clock mode.

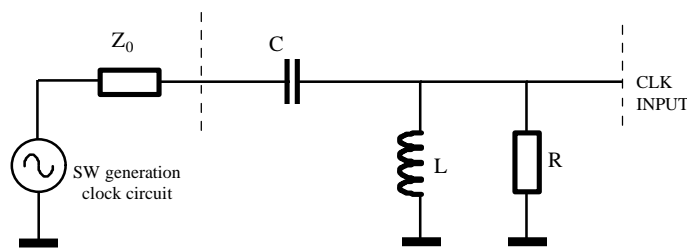
Note 1 : On the diagram of the Figure 11, the suppression of the inductance L allows to obtain directly the TTL clock compatibility. In this case, the TTL threshold is internally restored on CLKN pin which must be bypassed to ground with decoupling capacitor of 100 nF.

Note 2 : Another option for AC-coupling is shown on the diagram **Figure 13**.



- FIGURE 13 -

The dynamic equivalent clock input circuit is shown on the hereunder diagram :

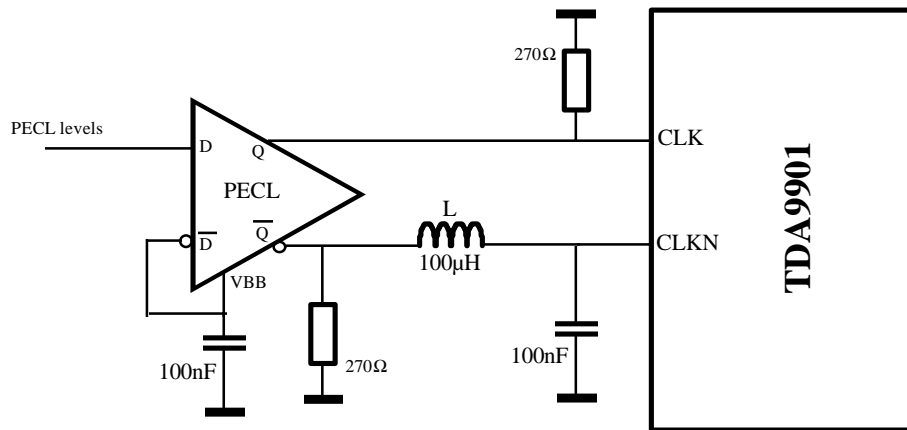


At the frequency clock F_c , the following condition must be repeated :

$$\frac{1}{C\omega_c} \ll |Z_{IN}| \quad \text{with,} \quad |Z_{IN}| = \frac{R L \omega_c}{\sqrt{R^2 + L^2 \omega_c^2}}$$

Therefore, if the value of the resistor R is sufficiently high, the inductance value L will can be choose in order to obtain the matching impedance on the output generation clock circuit.

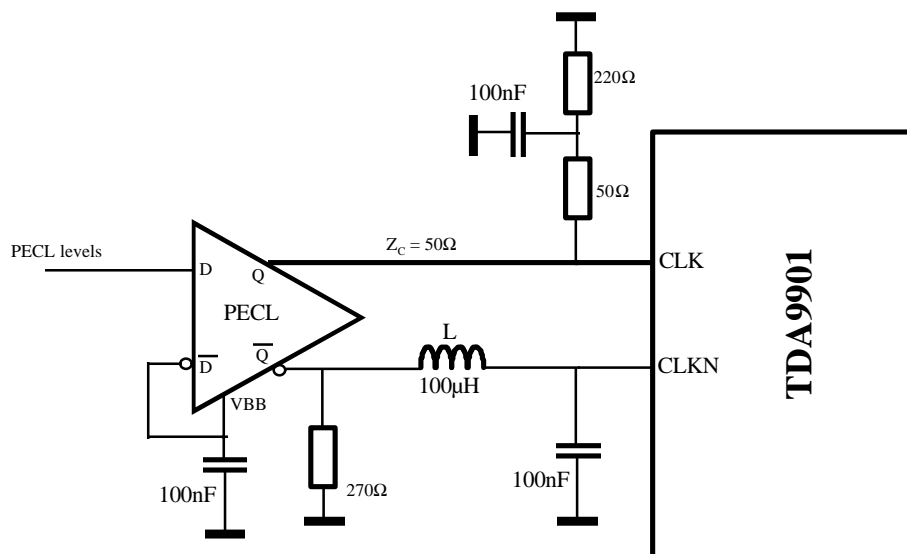
Note 3 : Use Pseudo-ECL (*PECL*) as interfacing single-ended clock circuit is possible as shown **Figure 14**, where a PECL trceiver used to drive the clock signal to DPGA.



- FIGURE 14 -

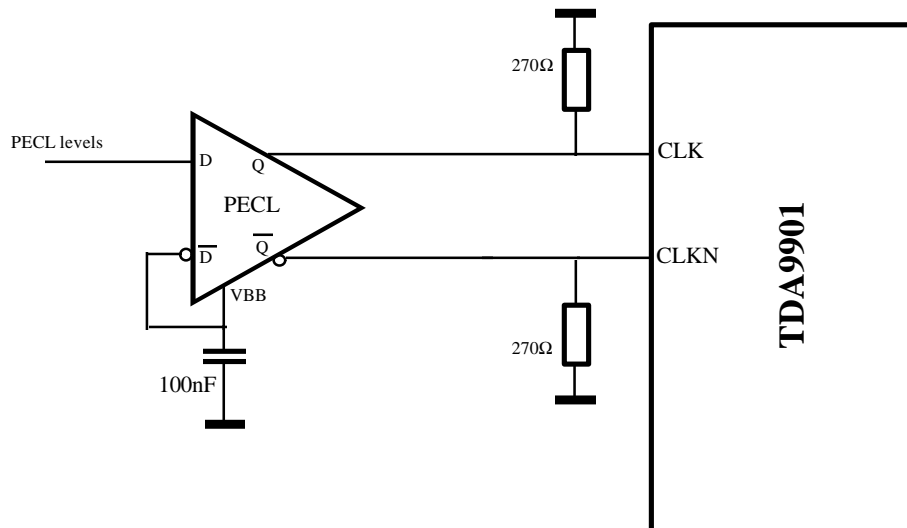
The PECL trceiver is fully powered under +5V and the active PECL output load will must be placed close to CLK pin of the DPGA. The offset voltage is restored on CLKN pin through the inductance L ($100\mu H$) and the decoupling capacitor ($100nF$) from complementary PECL output.

Nevertheless, a such practical configuration can be made when the transmission line, between PECL output and CLK pin, will be lower than one inch. Beyond, the transmission line will match to 50Ω dynamic load as shown on the diagram of the **Figure 15**.



- FIGURE 15 -

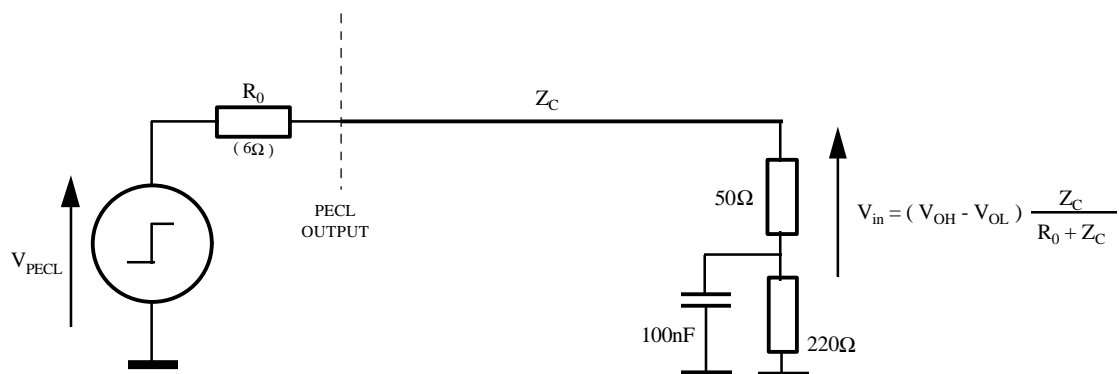
Note 4 : A differential PECL clock mode can be also used to drive the DPGA clock input as shown **Figure 16**.



- FIGURE 16 -

A low skew PECL trceiver can be employed to transfer directly the PECL levels from output trceiver to differential clock inputs of the device. Nevertheless, in order to preserve a duty cycle low skew on the differential clock signal, the transmission lines will must be of same length and sufficiently short (*1 inch*). Moreover, in order to avoid the over/undershoots on the transient clock signals, the length open lines located between the PECL output load and the clock pins will must be reduced as possible.

Note 5 : If the practical configuration requires of long transmission lines, these must be 50Ω matched to dynamic PECL loads as before mentioned (*see note 3 and figure 15*). For each line the dynamic equivalent diagram is shown on the hereunder figure :

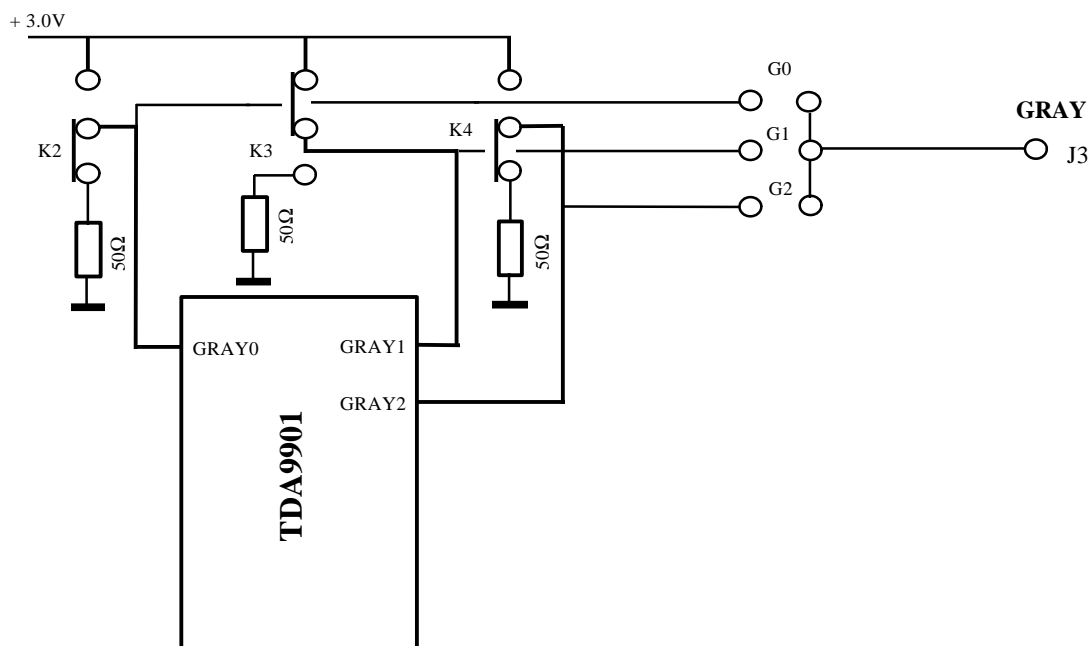


5.5 GRAY INPUT

On the Demonstration-Board, the DPGA can be switched between two consecutive gains only with a difference of $\pm 6\text{dBV}$ between 6 to 30dBV value. Thereby, three Low Voltage CMOS compatible Gray code inputs GRAY0, GRAY1 and GRAY2 pins are specially provided on the device. So, as shown on **Figure 17**, thanks to three switches (*K2 to K4*) a static level DVCC (3V) or GROUND (0V through 50W resistor) according to hereunder Gray coding table, is applied on each GRAY input (*GRAY0, GRAY1 and GRAY2*) to fix a particular gain value. **In this case the gain value can be fixed or changed manually only and no dynamic signal is applied on 50Ω SMA connector (J3).**

GRAY INPUT DATA CODE			GAIN (dB)
GRAY0	GRAY1	GRAY2	
0	0	0	6
1	0	0	12
1	1	0	18
0	1	0	24
0	1	1	30

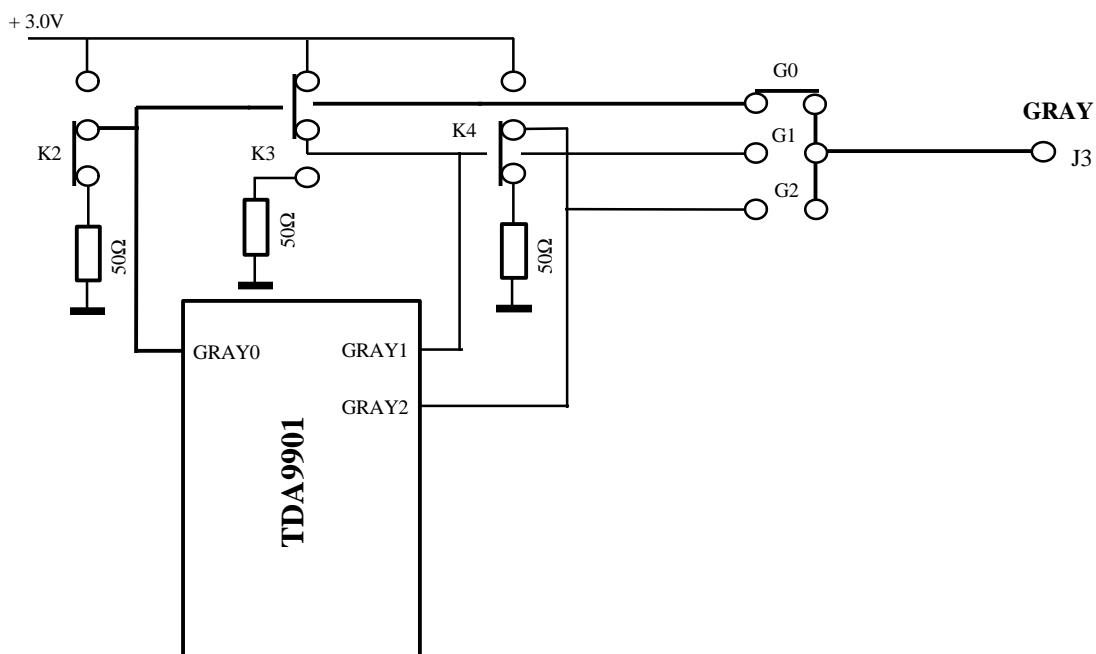
For example, Figure 17 a differential gain of 24dBV is programmed, by a changing position of K2 the gain will be reduced of 6dB. In the same way, if the position of K3 change, the gain value increase of 6dB.



- FIGURE 17 -

On the other hand, a change gain can be also obtained dynamically from a low frequency LV-CMOS compatible signal applied on GRAY SMA input (*J3*). Indeed, this signal can be driven to one GRAY input among the three of the device (*GRAY0*, *GRAY1* and *GRAY2*) thanks to a specific contact G0, G1 or G2.

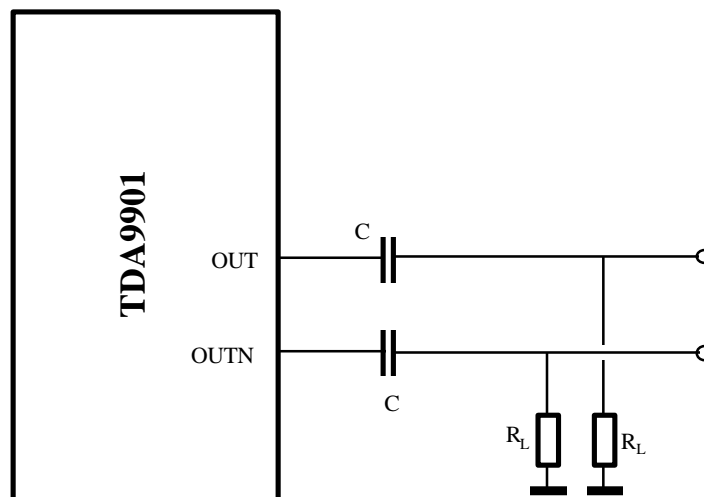
Nevertheless, in this condition, the switched GRAY input must be imperatively shorted to 50Ω thanks to the relevant switch as shown on **Figure 18** where a change gain of 18 to 24 dBV is obtained, by changing dynamically the level on GRAY0 input pin.



- FIGURE 18 -

5.6 ANALOG OUTPUT

On the Demonstration-Board, the output DC voltage is about 2.7V. The AC coupled outputs are loaded by minimum resistor of 680Ω referenced to the ground (*higher value can be also used*), as shown on **Figure 19**.



- FIGURE 19 -

In this condition, the maximum dynamic single-ended output signal available on each High Impedance SMA connector is : $1V_{p-p}$.

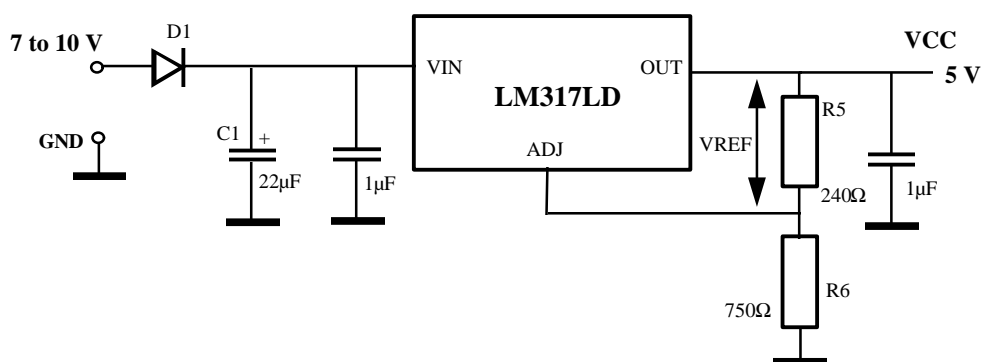
The combination of the capacitor C and the resistor load R_L form a high-pass filter whose the -3dB cut-off frequency is determined by following equation : $F_{-3dB} = 1 / 2 \pi R_L C$.

Note : To limit the large analog bandwidth of the DPGA an output band-pass filter can be added. In this case, the specified output impedance of the DPGA (*typical value of 15Ω*) must be taken into account to design the output filter.

6. GENERAL POWER SUPPLY

The proposed electrical diagram is shown **Figure 20**. This circuit uses a low current adjustable voltage regulator type LM317LD of SGS-Thomson in SMD package SO8. This one allows to obtain the voltage VCC necessary to supply the VDDA and VDDD from an external power unit of 9V/0.5A, (*the external voltage can be comprised between 7 and 10 Volts*).

The SMD type BYD17G Silicium diode D1 ensures protection for all circuitry from reverse polarities and C1 ensures a low frequency decoupling made before the supply line network distributed to regulators. Under the external power supply nominal value + 9 Volts, the consumption is lower than 200mA.



- FIGURE 20 -

In order to obtain a Low voltage value of VCC the value of the resistor R6 must satisfy the following relation :

$$VCC = V_{REF} \cdot \frac{R5 + R6}{R5}$$

with $R4 = 240\Omega$ fixed we obtain :

$$R6 = R5 \cdot \left(\frac{VCC}{V_{REF}} - 1 \right) \quad \text{thus,} \quad R6 = 750 \, \Omega$$

The input and output decoupling capacitors of 1µF were implanted close to the respective pin of the regulator.

7. PERFORMANCES

An evaluation of the performances of the TDA9901 Digital Programmable Gain Amplifier has been made on the dynamic test bench, with Demonstration Board environment.

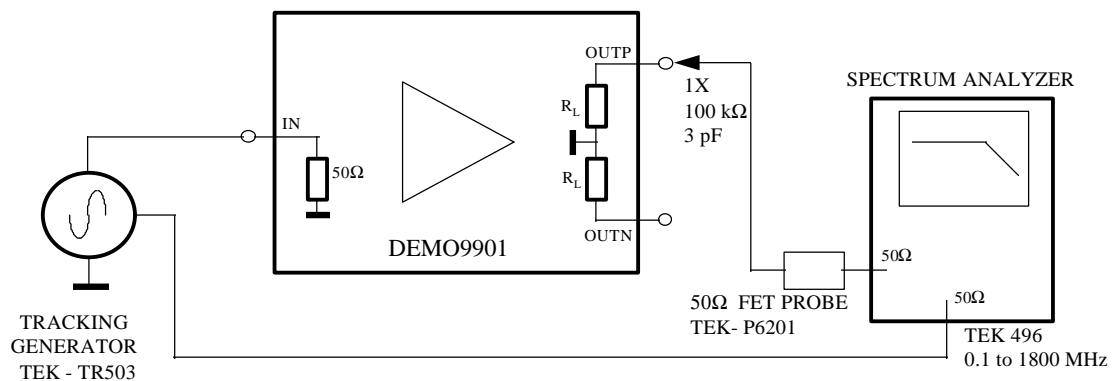
7.1 LOW SIGNAL BANDWIDTH

An evaluation has been made for all gain values with the following conditions and measurement set-up shown **Figure 21** :

Analog input signal : $V_{IN} = -30 \text{ dBm} = \text{Cte}$

Dynamic output load : $R_L = 680 \text{ W}$

Measurement : *Output single mode*



- FIGURE 21 -

The results obtained at -3 dB cut-off-frequency are mentioned on the hereunder table :

Programmed Gain position (dBV)	Single Output Gain (dBV)	Bandwidth (MHz)
6	0	125.0
12	6	
18	12	
24	18	
30	24	

The low signal bandwidth is totally independent of the Amplifier Gain value.

7.2 HARMONIC DISTORTION

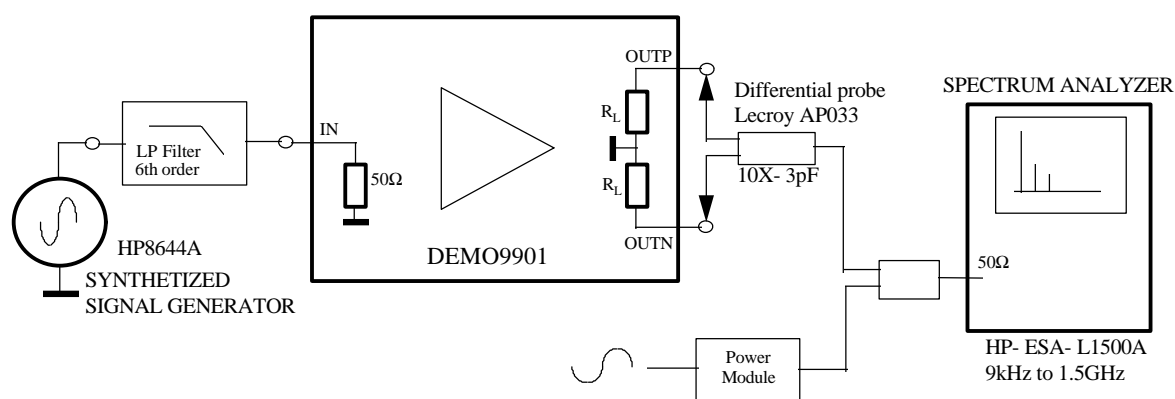
The measurement set-up used to evaluate the Harmonic Distortion of the DPGA is shown on **Figure 22**, and the measurement conditions are the following :

Analog single output signal : $V_o = 1 V_{p-p} = Cte.$

Gain position : $24dBV$

Dynamic output load : $R_L = 680W$

Measurement : *Output differential mode.*



- FIGURE 22 -

The results obtained on the second and third harmonics of the different analog frequencies up to 20MHz are mentioned in the below table :

F_{IN} (MHz)	H2 (dB)	H3 (dB)
0.50	- 69.9	- 71.0
4.43	- 73.8	- 64.0
12.50	- 74.7	- 64.5
21.40	- 72.2	- 71.5

The Harmonic Distorsion performances are guaranted for all gain positions and $2V_{p-p}$ differential output signal up to about 20MHz, only.

7.3 LATCHED MODE TIMING DIAGRAM

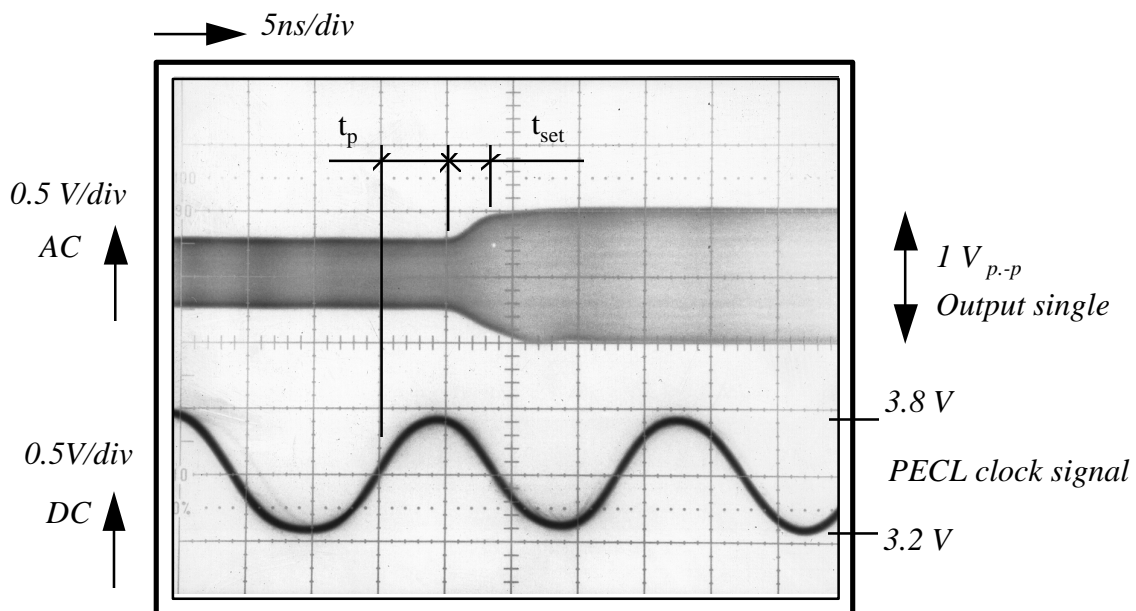
The timing diagram obtained with the following measurement conditions is shown on **Figure 23**.

Analog frequency : $F_{IN} = 4.43 \text{ MHz}$

Clock frequency : $F_{CLK} = 52 \text{ MHz}$

Gray frequency : $F_{GRAY} = 200 \text{ kHz}$

Output signal : $V_0 = 1 \text{ V}_{p-p}$



- FIGURE 23 -

For all changing gain, in latched mode ($TE = 0$) the gain change is fixed at the rising edge of the clock input and the different timing obtained are the following :

Propagation delay time : $t_p = 5.1 \text{ ns}$

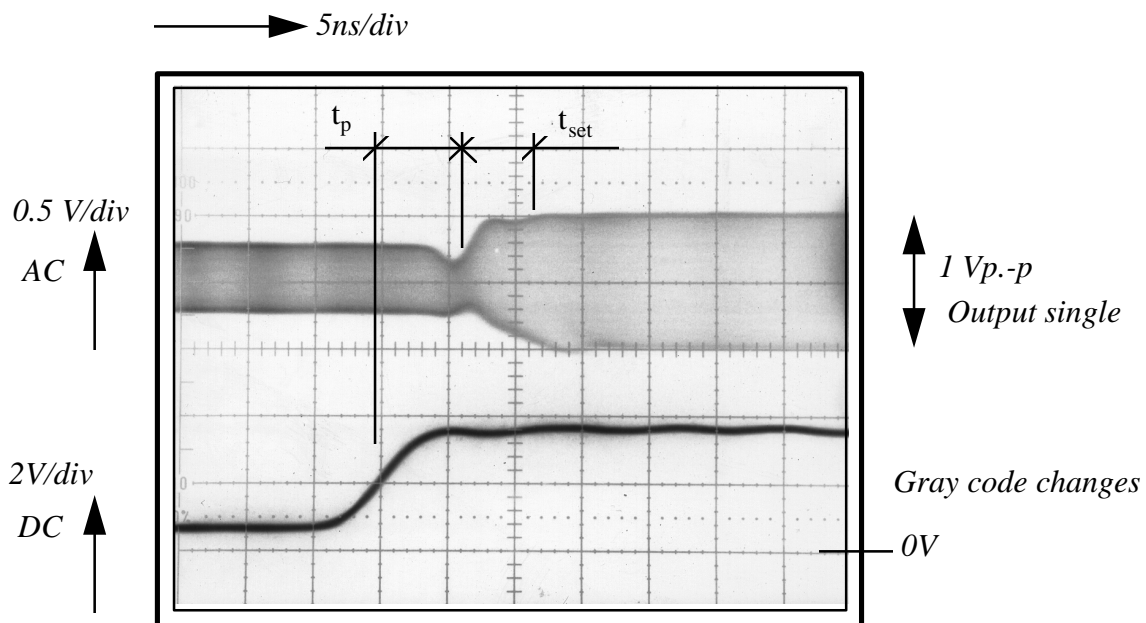
Gain settling time : $t_{set} = 3 \text{ ns}$

7.4 TRANSPARENT MODE TIMING DIAGRAM

The timing diagram obtained with the following measurement conditions is shown on **Figure 24** (for 0 to 6dBV gain changes) and **Figure 25** (for 18 to 24dBV gain changes):

Analog frequency : $F_{IN} = 4.43 \text{ MHz}$ Gray frequency : $F_{GRAY} = 200 \text{ kHz}$

Output signal : $V_0 = 1 \text{ V}_{p-p}$ (single mode)



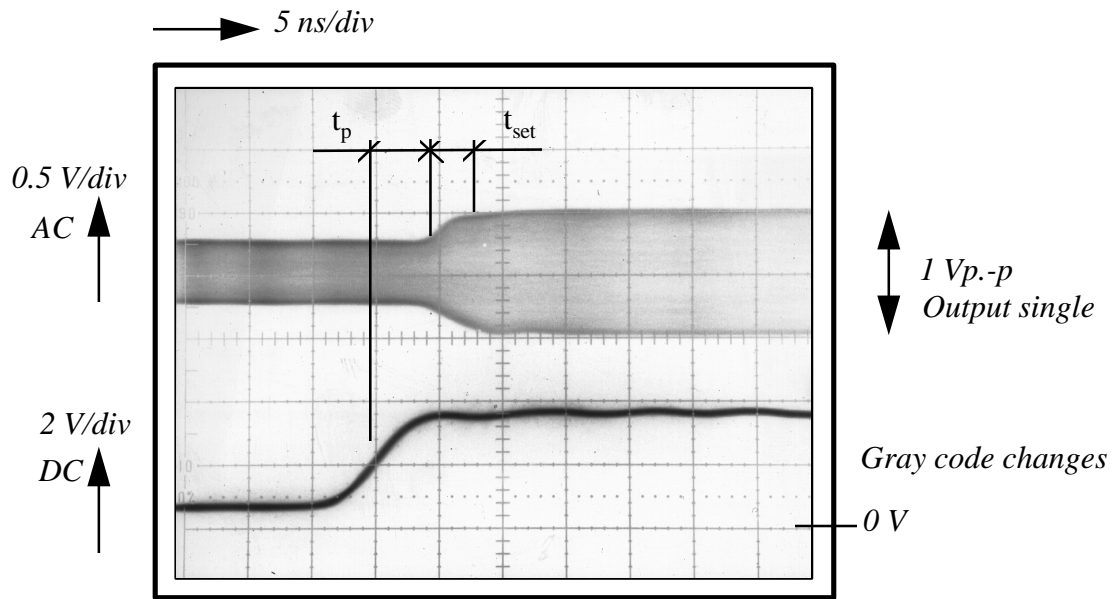
Transparent mode : Gain changes 0 to 6 dBV

- FIGURE 24 -

In transparent mode ($TE = 1$), the gain settling is directly controlled by the input Gray data pattern. For a changing gain of 0 to 6dBV (or 6 to 12dBV in output differential mode) the different timings obtained are the following :

Propagation delay time : $t_p = 6.5 \text{ ns}$

Gain settling time : $t_{set} = 5.2 \text{ ns}$



Transparent mode : Gain changes 18 to 24dBV

- FIGURE 25 -

For a changing gain of 18 to 24dBV (or 18 to 30dBV in output differential mode) the different timings obtained are the following :

Propagation delay time : $t_p = 5.0 \text{ ns}$

Gain settling time : $t_{set} = 4.0 \text{ ns}$

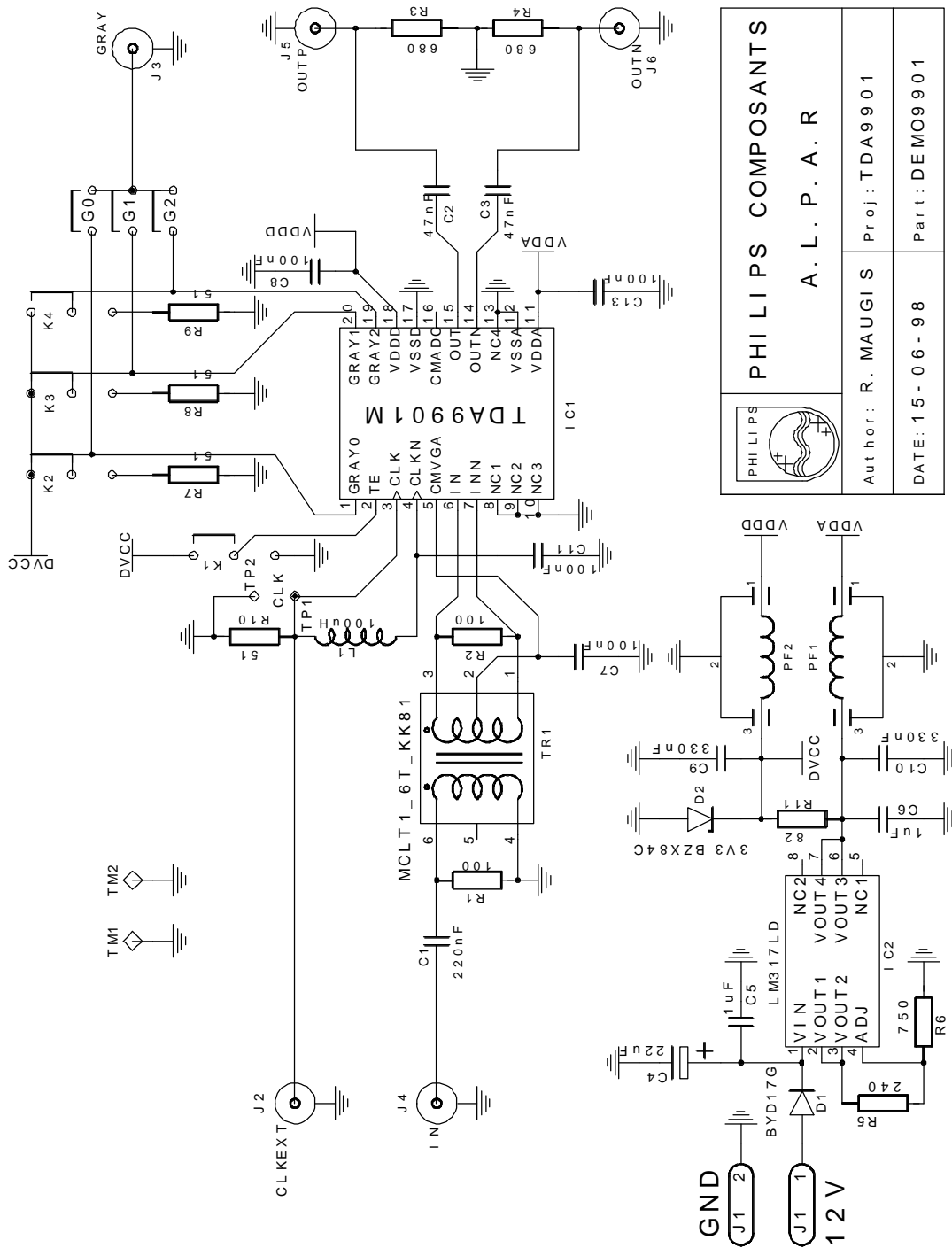
8. DEMO-BOARD FILE


The following documents are shown on **Figures 26 to 32**:

- Electrical diagram.
- Double sided layout.
- Internal ground planes.
- Internal layer supply layout.
- Double sided components implantation.

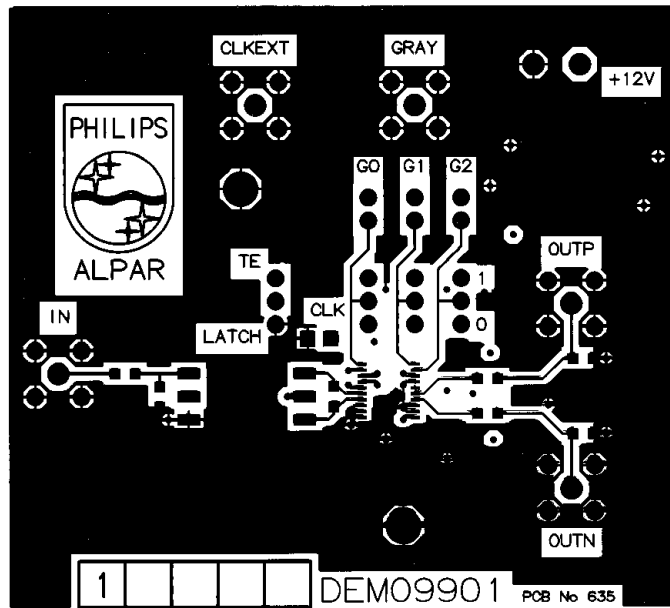
The part list with the values and references of all components is given in the **Table1**.

TDA9901 - Digital Programmable Gain Amplifier
DEMONSTRATION BOARD



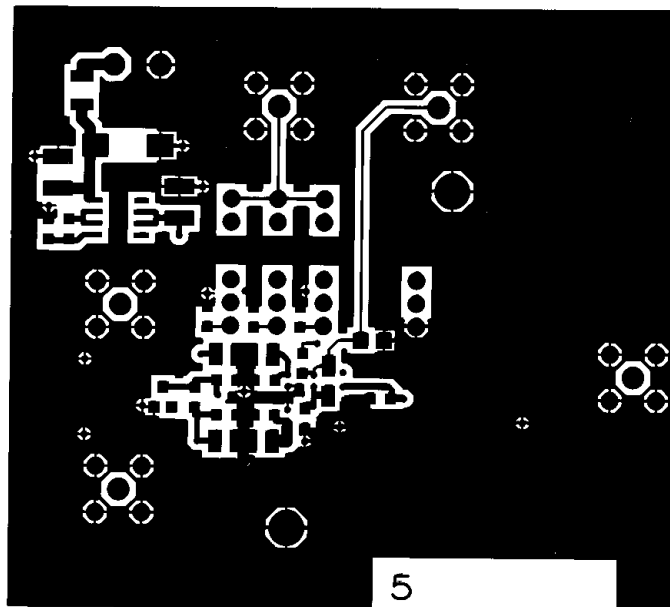
	PHILIPS COMPONENTS		
	A. L. P. A. R		
Author: R. MAUGIS	Proj: TDA9901		
DATE: 15-06-98	Part: DEMO9901		

- FIGURE 26 -



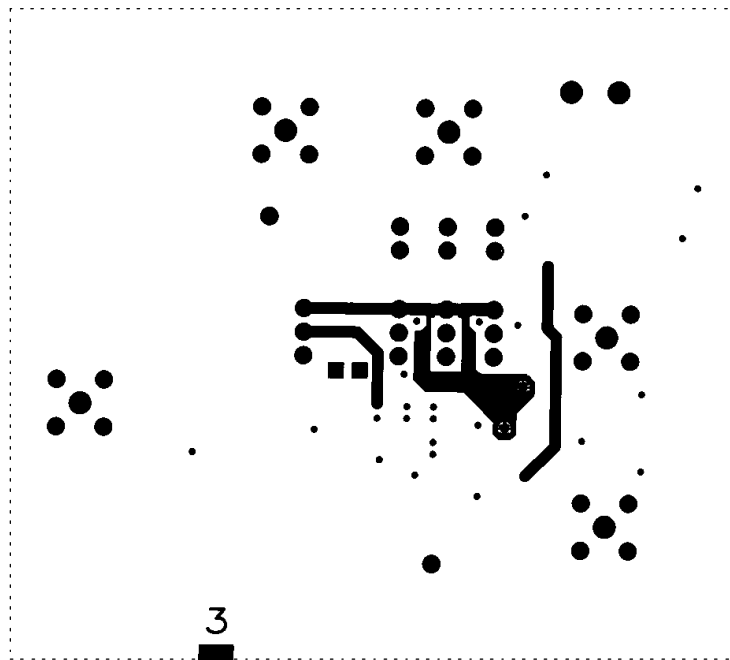
OVERSIDE LAYOUT

- FIGURE 27 -



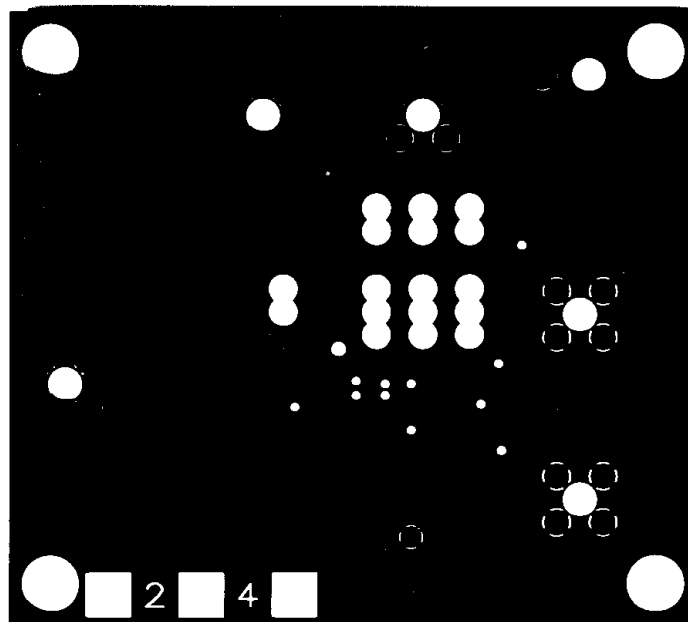
UNDERSIDE LAYOUT

- FIGURE 28 -



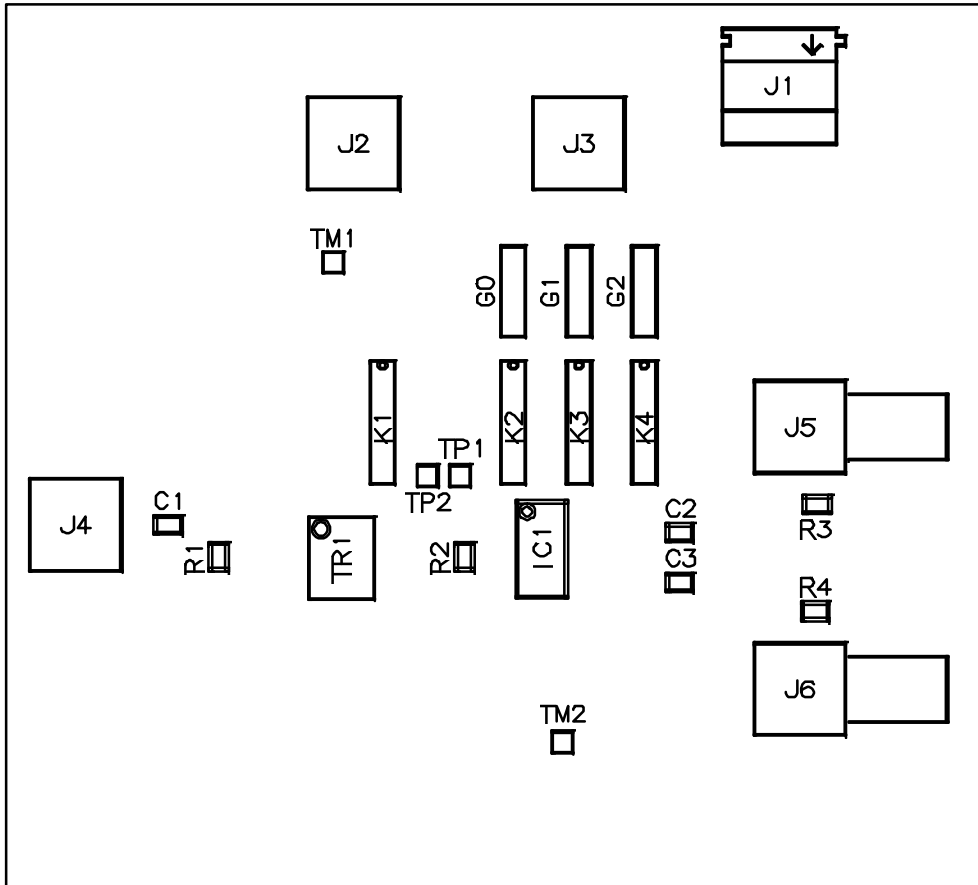
INTERNAL SUPPLY PLANE

- FIGURE 29 -



INTERNAL GROUND PLANES

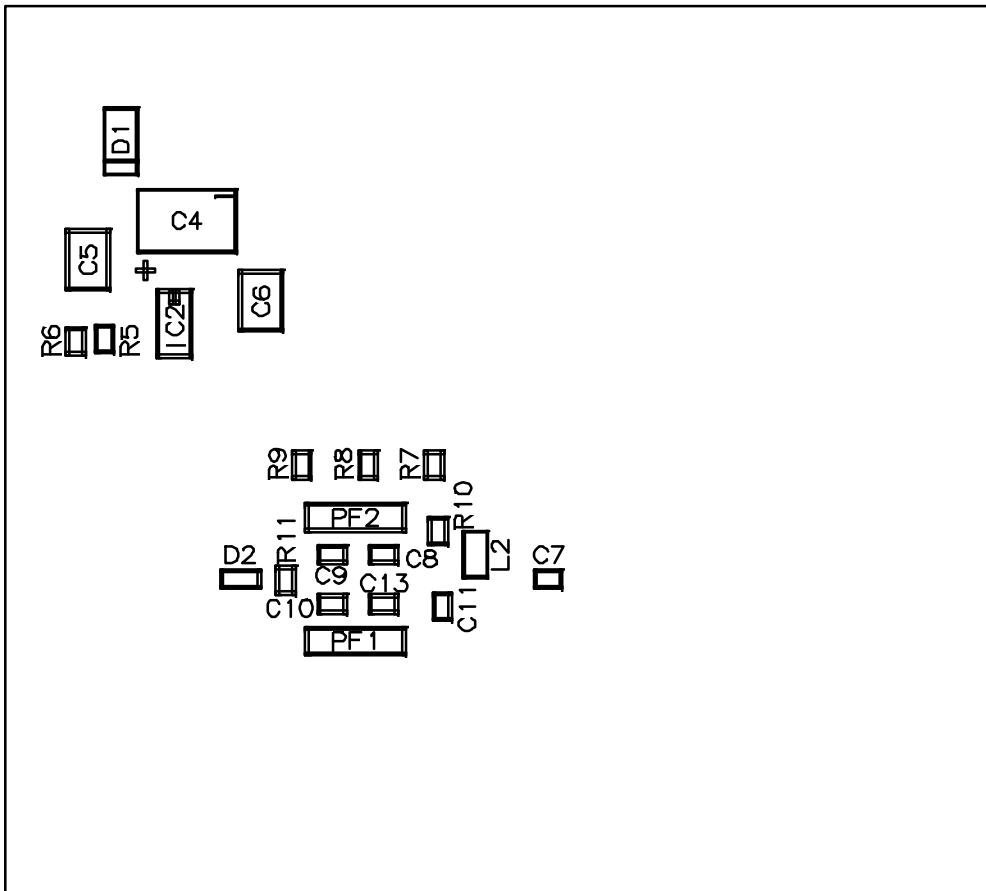
- FIGURE 30 -



DEM0990 1-635

OVERSIDE COMPONENTS IMPLANTATION

- FIGURE 31 -



DEM09901-635

UNDERSIDE COMPONENTS IMPLANTATION

- FIGURE 32 -

REFERENCES	VALUES	CODE NUMBER	MANUFACTURER
IC1	AMPLIFIER	TDA9901	PHILIPS
IC2	REGULATOR	LM 317LD	SGS-THOMSON
D1	SMD DIODE	BYD17G	PHILIPS
D2	SMD ZENER DIODE	BZX84C/3V3	-
TR1	RF TRANSFORMER	MCLT1-6T-KK81	MINI CIRCUIT
BP1	PI FILTER 2nF	4700- 003-S	TUSONIX
BP2	-	-	-
L1	SMD SELF 100 μ H	LQH1N101K04	MURATA
J1	EDGE	MKSD 1.5/2-5.08	PHOENIX CONTACT
J2 to J4	50 Ω -SMA	R125 426	RADIALL
J5 - J6	-	R125 680	-
K1 to K4	SWITCH 1C/2P	09 03201 02	SECME
G0 to G2	2.54 - STRAP	M7566-06	HARWIN
TP1 - TP2	TEST POINT	3850358102400	COMATEL
TM1 TM2	BOLT HOLD	3110415000530	-
C1	SMD 220nF	C0805	PHILIPS
C2 - C3	SMD 47nF	-	-
C4	22 μ F/16V	293D226X9016D	SPRAGUE
C5 - C6	SMD 1 μ F	C1812	PHILIPS
C7 - C8	SMD 100nF	C0805	-
C9 - C10	SMD 330nF	-	-
C11 - C13	SMD 100nF	-	-
R1 - R2	SMD 100 Ω	0805	PHILIPS
R3 - R4	SMD 680 Ω	-	-
R5	SMD 240 Ω	-	-
R6	SMD 750 Ω	-	-
R7 to R10	SMD 51 Ω	-	-
R11	SMD 82 Ω	-	-

- TABLE 1 -